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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,795	08/21/2003	Akira Morita	116915	7417

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,795	MORITA ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicants' cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. At least figures 1-4A, 4B, 10A, and 10B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurokawa et al (US 6,130,657 A).

Regarding claim 1, Kurokawa discloses a display driver circuit [Fig. 1; ICBLK] which drives signal electrodes [Fig. 1; Y] of a display device [Fig. 5; LCD] based on gray-scale data [Fig. 1; DATA], comprising: first to (M+N)th (M and N are positive integers) shift register blocks [Fig. 1; 301]; a data input control circuit [Fig. 1; 307] which controls input of the gray-scale data supplied to the first to (M+N)th shift register blocks; first to (M+N)th data mask circuits [Fig. 1; 305] which generate first to (M+N)th gray-scale data by performing mask control for the gray-scale data supplied to the first to (M+N)th shift register blocks and output the first to (M+N)th gray-scale data; and a signal electrode driver circuit [Fig. 1; ICBLK] which drives the signal electrodes by using drive voltages corresponding to the first to (M+N)th gray-scale data, the first to (M+N)th gray-scale data being held in the first to (M+N)th shift register blocks [Fig. 1; $301_{ICBLK1\text{-}3}$], wherein the first to Mth shift register blocks are disposed in a region on a first direction side [Fig. 1; left side] of the data input control circuit, shift a given data enable signal input [Fig. 1; CAR1] to the first shift register block [Fig. 1; 301_{ICBLK1}] and output the shifted data enable signal to a shift register block [Fig. 1; 301_{ICBLK2}] adjacent in a second direction [Fig. 1; to the right] opposite to the first direction, and hold the first to Mth gray-scale data based on the shifted data enable signal, wherein the (M+1)th to (M+N)th shift register

blocks [Fig. 1; $301_{ICBLK4-6}$] are disposed in a region on the second direction side [Fig. 1; right side] of the data input control circuit, shift a data enable signal input to the (M+1)th shift register block [Fig. 1; 301_{ICBLK4}] from the Mth shift register block [Fig. 1; 301_{ICBLK3}] and output the shifted data enable signal to a shift register block adjacent [Fig. 1; 301_{ICBLK5}] in the second direction [Fig. 1; to the right], and hold the (M+1)th to (M+N)th gray-scale data based on the shifted data enable signal, wherein the first to Mth data mask circuits [Fig. 1; 305(1-3)] are connected in the second direction in order from the first to Mth data mask circuit and mask the first to Mth gray-scale data in order from the first to Mth data mask circuit, and wherein the (M+1)th to (M+N)th data mask circuits [Fig. 1; 305(4-6)] are connected in the second direction in order from the (M+1)th to (M+N)th data mask circuit and unmask the (M+1)th to (M+N)th gray-scale data in order from the (M+1)th to (M+N)th data mask circuit (see Column 4, Line 15 - Column 5, Line 47).

Regarding claim 2, Kurokawa discloses first to (M+N)th data mask control circuits [Fig. 1; 306] which generate first to (M+N)th data mask control signals [Fig. 1; SSD] for performing mask control for the first to (M+N)th gray-scale data, wherein an ath ($1 \leq a \leq M$; a is an integer) data mask control circuit [Fig. 1; 306(3)] generates an ath data mask control signal [Fig. 1; SSD(3)] based on a data enable signal [Fig. 1; CAR1] output from an ath shift register block [Fig. 1; 301_{ICBLK1}], and wherein a bth ($M+1 \leq b \leq M+N$; b is an integer) data mask control circuit [Fig. 1; 306(4)] generates a bth data mask control signal [Fig. 1; SSD(4)] based on a data enable signal output [Fig. 1; CAR2] from a (b-1)th shift register block [Fig. 1; 301_{ICBLK6}] (see Column 4, Line 43 - Column 5, Line 47).

Regarding claim 3, Kurokawa discloses a cth (1 ≤c ≤M+N; c is an integer) shift register block [Fig. 1; 301_{ICBLK1}] shifts a data enable signal in the first direction and holds a cth gray-scale data based on the data enable signal shifted in the first direction, when a given shift signal is at a first level , wherein the cth shift register block shifts a data enable signal in the second direction and holds the cth gray-scale data based on the data enable signal shifted in the second direction, when the shift signal is at a second level, and wherein a cth data mask control circuit generates a cth data mask control signal according to the level of the shift signal (see Fig. 2; Column 4, Lines 36-42).

Regarding claim 4, Kurokawa discloses a clock input control circuit [Fig. 1; 307] which controls input of a clock signal [Fig. 1; CL] which is supplied to each of the first to (M+N)th shift register blocks and determines shift timing of a data enable signal [Fig. 1; CAR]; and first to (M+N)th clock mask circuits [Fig. 1; 305] which generate first to (M+N)th clock signals [Fig. 1; SSSCL2] by performing mask control for the clock signal supplied to the first to (M+N)th shift register blocks and output the first to (M+N)th clock signals, wherein the first to Mth shift register blocks are disposed in the region on the first direction side of the clock input control circuit and shift a data enable signal [Fig. 1; CAR1] based on the first to Mth clock signals [Fig. 1; SSSCL2(1-3)], wherein the (M+1)th to (M+N)th shift register blocks are disposed in the region on the second direction side of the clock input control circuit and shift a data enable signal [Fig. 1; CAR2] based on the (M+1)th to (M+N)th clock signals [Fig. 1; SSSCL2(4-6)], wherein the first to Mth clock mask circuits are connected in the second direction in order from the first to Mth clock mask circuit and mask the first to Mth clock signals in order from the first to Mth clock mask circuit, and wherein the (M+1)th to (M+N)th clock mask circuits are connected in

the second direction in order from the (M+1)th to (M+N)th clock mask circuit and unmask the (M+1)th to (M+N)th clock signals in order from the (M+1)th to (M+N)th clock mask circuit (see Column 4, Line 15 - Column 5, Line 47).

Regarding claim 5, Kurokawa discloses first to (M+N)th clock mask control circuits [Fig. 1; 306] which generate first to (M+N)th clock mask control signals [Fig. 1; SSCL2] for performing mask control for the first to (M+N)th clock signals, wherein a dth ($1 \leq d \leq M$; d is an integer) clock mask control circuit [Fig. 1; 306(3)] generates a dth clock mask control signal [Fig. 1; SSCL2(3)] based on a data enable signal [Fig. 1; CAR1] output from a dth shift register block [Fig. 1; 301_{ICBLK1}], and wherein an eth ($M+1 \leq e \leq M+N$; e is an integer) clock mask control circuit [Fig. 1; 306(4)] generates an eth clock mask control signal [Fig. 1; SSCL2(4)] based on a data enable signal [Fig. 1; CAR1] output from an (e-1)th shift register block [Fig. 1; 301_{ICBLK6}] (see Column 4, Line 15 - Column 5, Line 47).

Regarding claim 6, Kurokawa discloses an fth ($1 \leq f \leq M+N$; f is a positive integer) shift register block [Fig. 1; 301_{ICBLK1}] shifts a data enable signal [Fig. 1; CAR1] in the first direction and holds an fth gray-scale data [Fig. 1; SSSD(1)] based on the data enable signal shifted in the first direction, when a given shift signal is at a first level, wherein the fth shift register block shifts a data enable signal in the second direction and holds the fth gray-scale data based on the data enable signal shifted in the second direction, when the shift signal is at a second level, and wherein an fth clock mask control circuit [Fig. 1; 306(1)] generates an fth clock mask control signal according to the level of the shift signal (see Fig. 2; Column 4, Lines 36-42).

Regarding claim 7, this claim is rejected by the reasoning applied in rejecting claims 1 and 4.

Regarding claim 8, this claim is rejected by the reasoning applied in rejecting claim 1.

Regarding claim 9, this claim is rejected by the reasoning applied in rejecting claim 1.

Regarding claim 10, this claim is rejected by the reasoning applied in rejecting claims 1 and 4.

Regarding claim 11, this claim is rejected by the reasoning applied in rejecting claims 1 and 4.

Regarding claim 12, Kurokawa discloses pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other; a scan electrode driver circuit [Fig. 5; IC-C] which drives the scan electrodes; and the display driver circuit [Fig. 5; IC-U & IC-L] driving the signal electrodes based on the gray-scale data (see Column 1, Lines 19-39).

Regarding claim 13, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 15, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 16, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 17, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 18, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 19, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 20, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 21, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 22, this claim is rejected by the reasoning applied in rejecting claim 12.

Regarding claim 23, this claim is rejected by the reasoning applied in rejecting claim 12.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Ikeda et al (US 6,222,518 B1), Imamura (US 5,726,677 A), Kawaguchi et al (US 5,602,561 A), Kusada (US 5,192,945 A), and Takeda (US 5,103,218 A) are cited to further evidence the state of the art pertaining to display driver circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
8 March 2006

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